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**Amendments to the claims**

Please cancel claims 63-75 and 81-96, all without prejudice, as indicated in the following listing of claims:

**Listing of Claims**

## Claims 1-75 (Cancelled)

76.(Previously Presented) A memory comprising:

an array cell having an output, an array threshold value set to one of n array threshold values to control a signal provided at the array cell output, and a gate;

a reference cell having an output, a floating gate which stores an electrical charge to allow a reference threshold value to be programmed, and a gate, the reference cell having its reference threshold value programmed between two successive ones of the n array threshold values to control a signal provided at the reference cell output;

a comparison circuit coupled to the array cell output and the reference cell output, the comparison circuit for comparing the signal at the array cell output to the signal at the reference cell output and providing a signal indicating which of the n array threshold values is held by the array cell; and

a power supply for supplying a supply voltage to the gate of the array cell to enable the array cell to provide the signal at the array cell output, the power supply further supplying the supply voltage to the gate of the programmable reference cell to enable the reference cell to provide the signal at the reference cell output.

77.(Previously Presented) The memory of claim 76 wherein when a value of the supply voltage is varied, a working margin between the array cell output and the reference cell output remains constant.

78.(Previously Presented) The memory of claim 76 wherein n is greater than two.

79.(Previously Presented) A memory comprising:

a first word line;

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a second word line;

a power supply for providing a substantially identical supply voltage to the first word line and the second word line;

an array cell having a gate connected to the first word line and a source-to-drain path, the array cell having a threshold value set to one of  $n$  array threshold values;

$n-1$  read reference cells, each read reference cell having a gate connected to the second word line, a source-to-drain path and a floating gate which stores an electrical charge to allow a reference threshold value to be programmed, each respective read reference cell having its reference threshold value programmed between two different successive ones of the  $n$  array threshold values; and

read sense amplifiers, each read sense amplifier having a first input coupled to the source-to-drain path of the array cell and a second input coupled to the source-to-drain path of a respective one of the read reference cells, each read sense amplifier for providing an output signal indicating whether a signal received at its first input is greater than a signal received at its second input.

80.(Previously Presented) The memory of claim 79 wherein  $n$  is greater than two.

Claims 81-96 (Cancelled)

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